Notice of Allowability	Application No.	Applicant(s)	
	09/998,325	TANI ET AL.	
	Examiner	Art Unit	
	Nitin Patel	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/30/2004*.

2. ☒ The allowed claim(s) is/are *10 and 12*.

3. ☒ The drawings filed on *03 December 2001* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Amare Mengistu
Primary Examiner

REASON FOR ALLOWANCE

1. Claims 10,12 are allowed. Claims 1-9,11,13-24 have been cancelled.

2. The following is an examiner's statement of reason for allowance:

The prior art fails to teach or suggest a display control device having a display memory which is capable of storing display data for the display device and into which display data are written in a prescribed number of bits at a time, the display control device successively reading the display data out of the display memory and forming and supplying a drive signal to the display device, wherein the display memory includes: a memory array provided with a plurality of memory cells arranged in a matrix form; a plurality of word lines to which selection terminals for the memory cells are connected, a plurality of bit lines which are arranged in a direction to cross the word lines and to which data input/output nodes for the memory cells are connected, input transfer means and output transfer means being connected to the bit lines, data transferring by the input transfer means resulting in writing of data into the memory sells connected to a word line in a selected state, and data transferring by the output transfer means resulting in reading of data out of the memory cells connected to the word line in a selected state and a plurality of first data latch means capable of successively taking in the display data in the prescribed number of bits at a time and display data held by the first data latch means can be collectively transferred by the input transfer to the bit lines of the display memory of the number of bits of the display data taken into the first data latch means, wherein the data processing unit generates display data to be written into the display memory and sets information on their writing position, the display device

carries out displaying with a display drive signal read out of the display memory and formed by the display control device based on the display data and the display control device having a segment drive for generating signals for driving segment electrodes of the display device and a common electrode drive circuit for generating a signal for driving common electrodes of the display device is configured as a semiconductor chip from a semiconductor chip over which the display control device is formed and the common electrode drive circuit is configured of an element higher in withstand voltage than the elements constituting the display control device as claimed in claim 10.

The prior art fails to teach or suggest a display control device formed over a single semiconductor substrate having a memory for storing display data to be displayed on a liquid crystal panel; a k-bit first external terminal to which display data to be stored in the memory are supplied from a microprocessor; a plurality of second external terminals for outputting drive signals for driving the liquid crystal panel on the basis of m-bit read data from the memory; a first latch circuit connected between the input of the memory and the first external terminal and capable of storing m-bit display data; a transfer circuit for selecting, for each integral multiple of the k bits, display data of not more than the m bits (k*n) in the first latch circuit and transferring them to bit lines of the memory and a second latch circuit provided between the transfer circuit and first latch circuit and capable of storing the m-bit display data, the second latch circuit outputting display data of the m bits (k*n) to the transfer circuit as claimed in claim 12.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 703-308-7024. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP

September 29, 2004

Amare Mengistu
Primary Examiner